

FIG.1

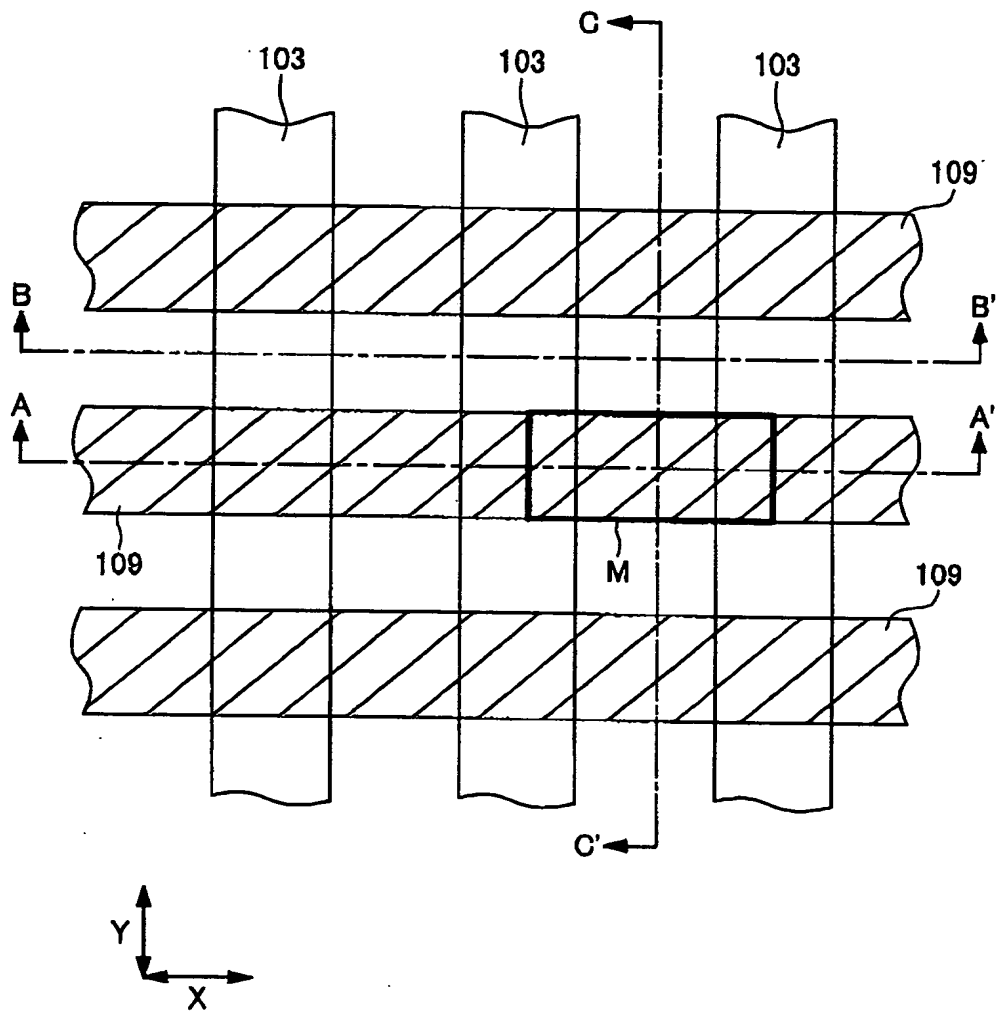


FIG.2

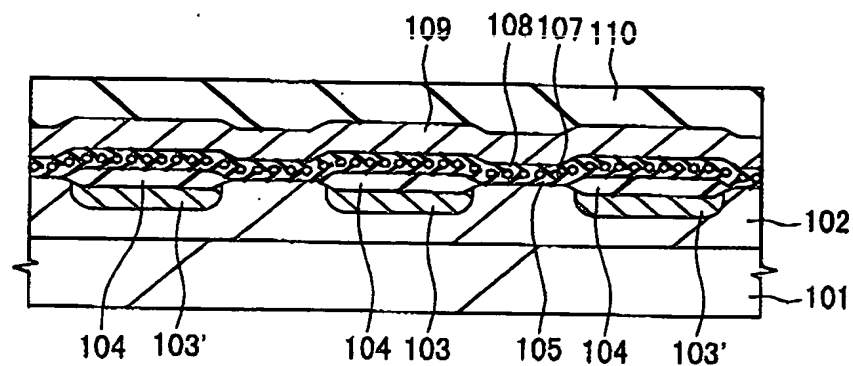


FIG.3

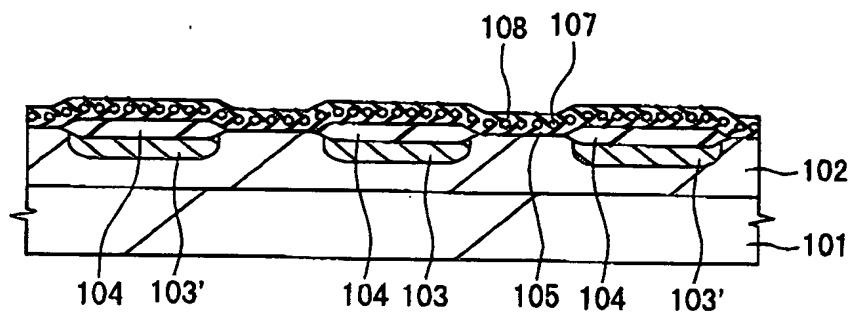


FIG.4

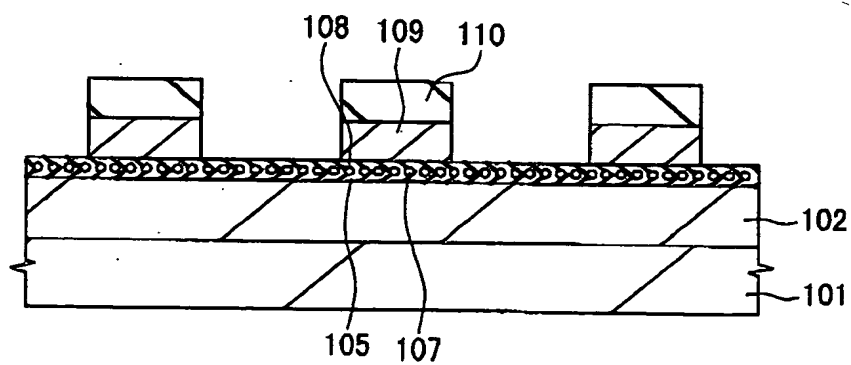
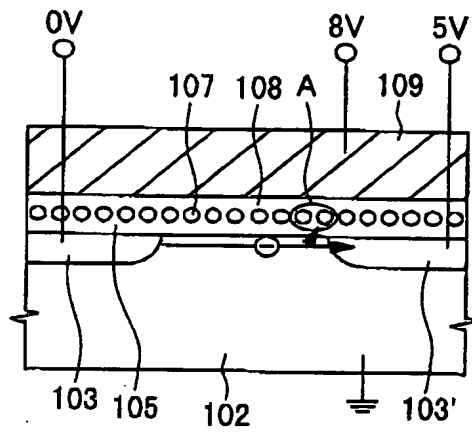
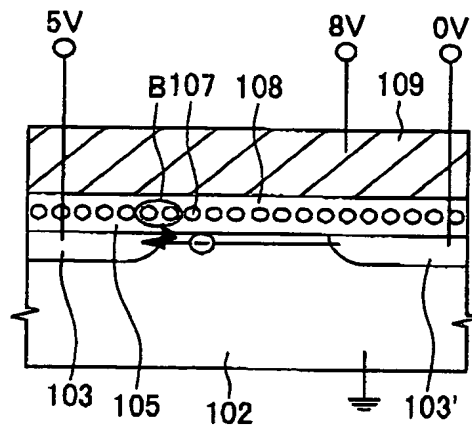


FIG.5



PROGRAM 1

FIG.6



PROGRAM 2

FIG.7

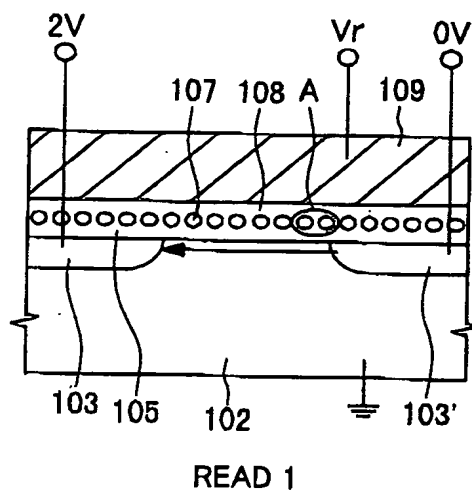


FIG.8

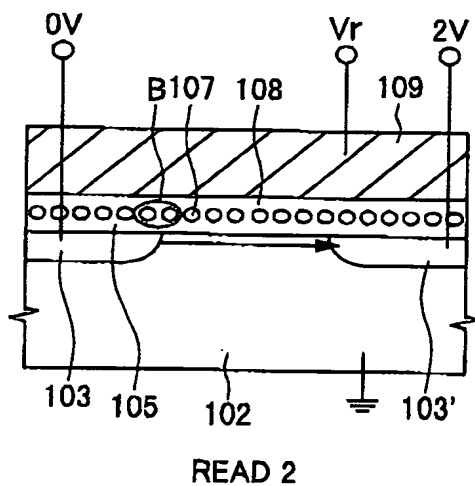


FIG.9

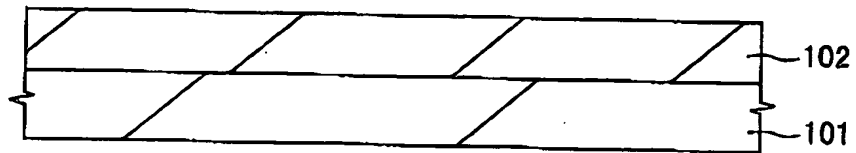


FIG.10

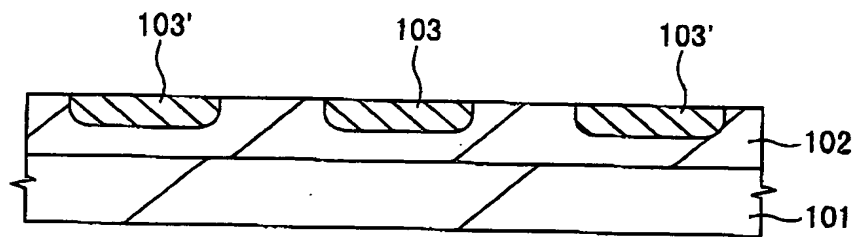


FIG.11

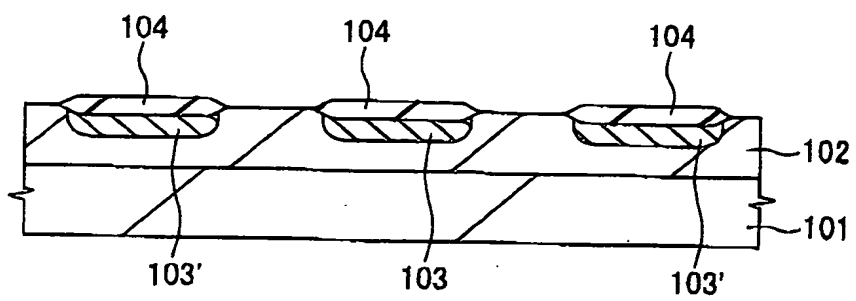


FIG.12

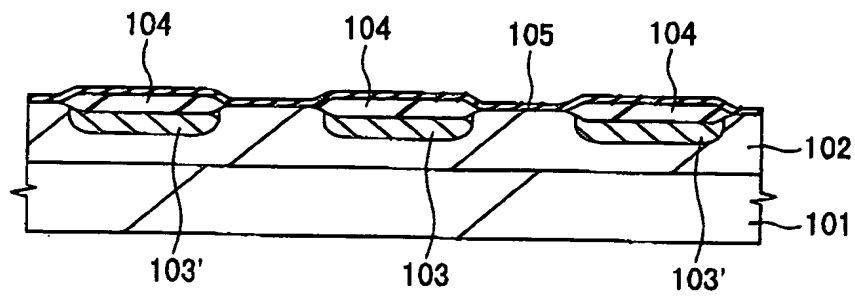


FIG.13

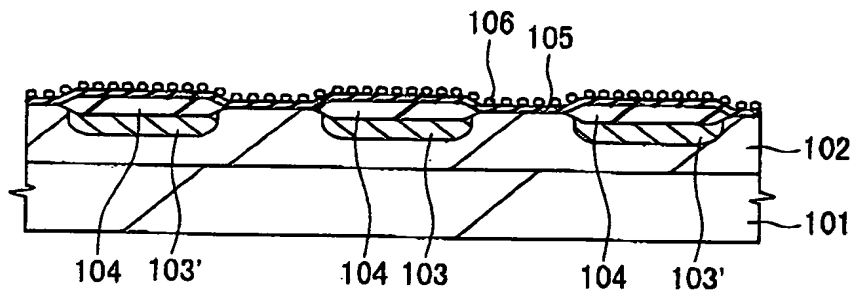


FIG.14

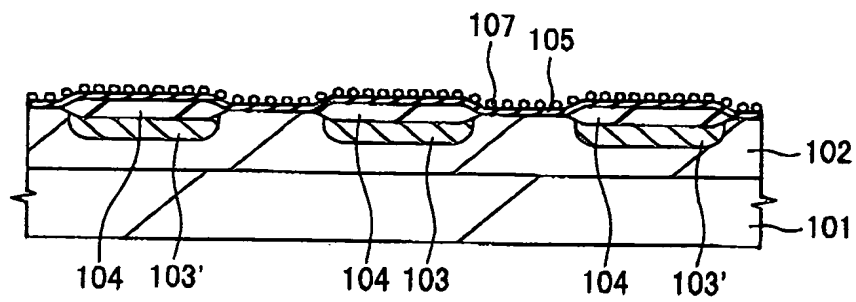


FIG.15

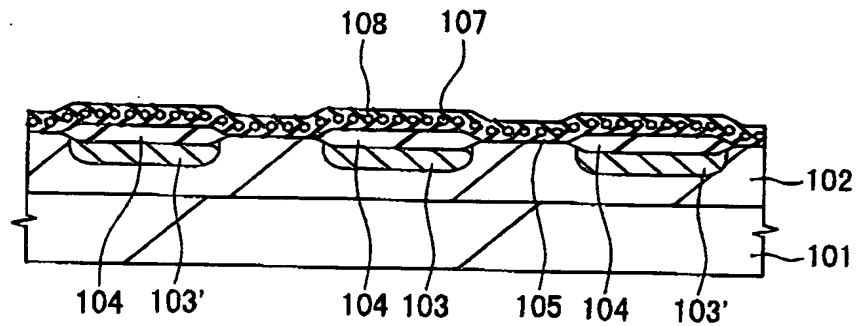


FIG.16

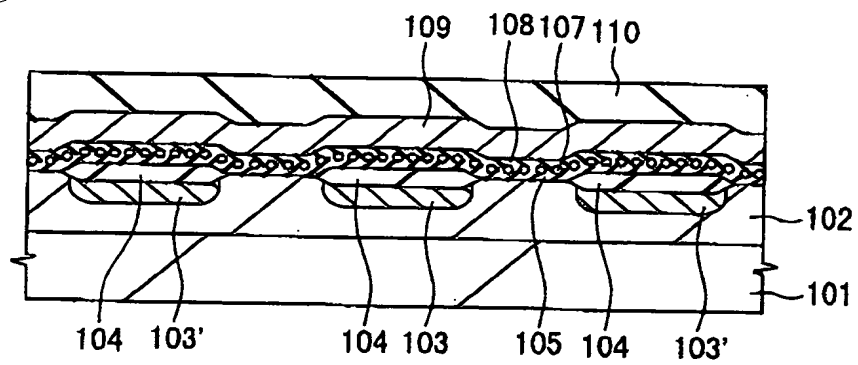


FIG.17

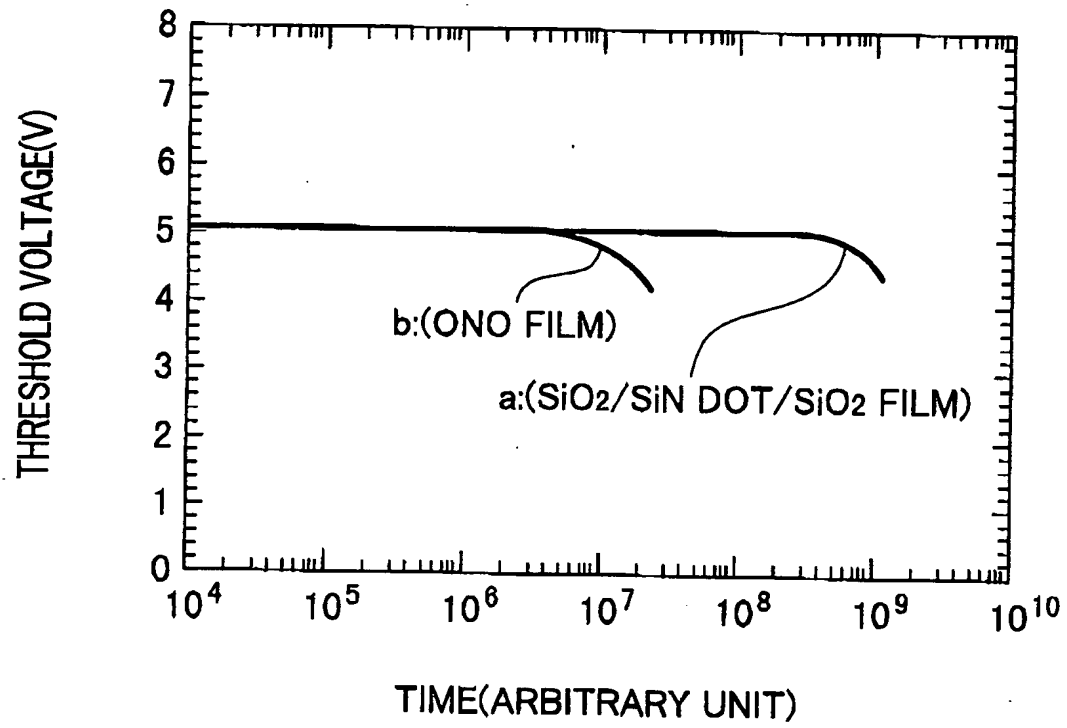


FIG.18

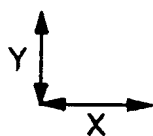
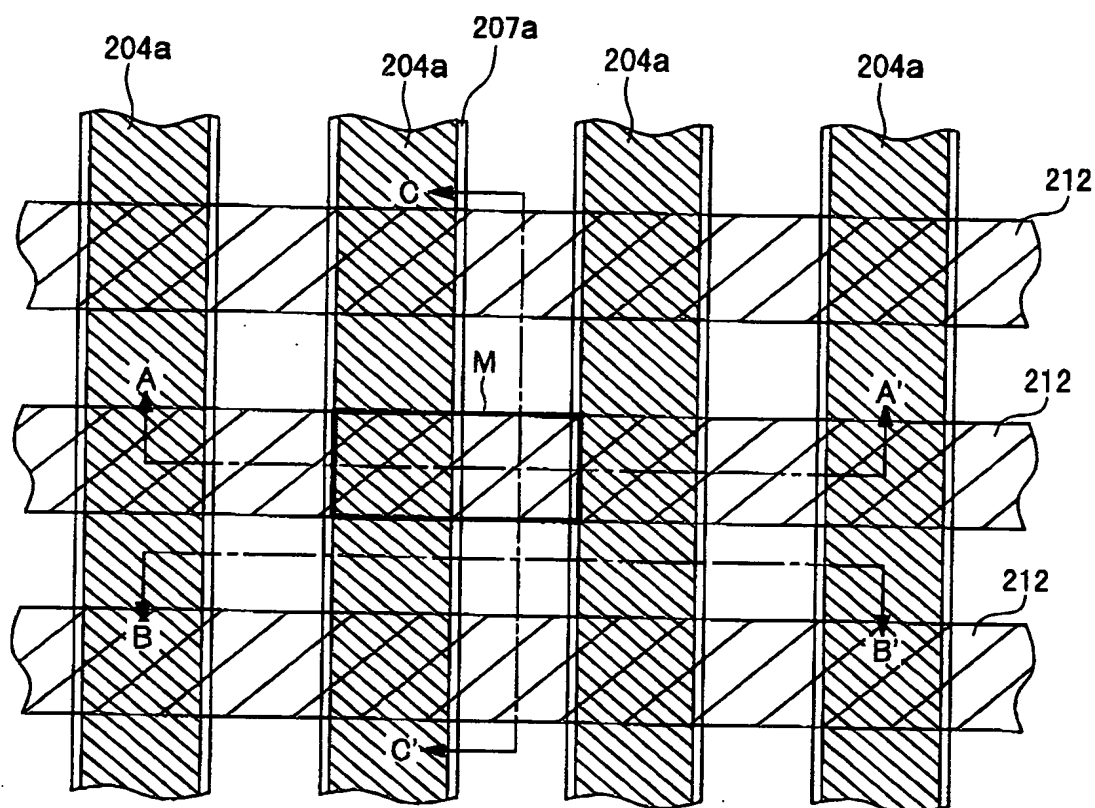


FIG.19

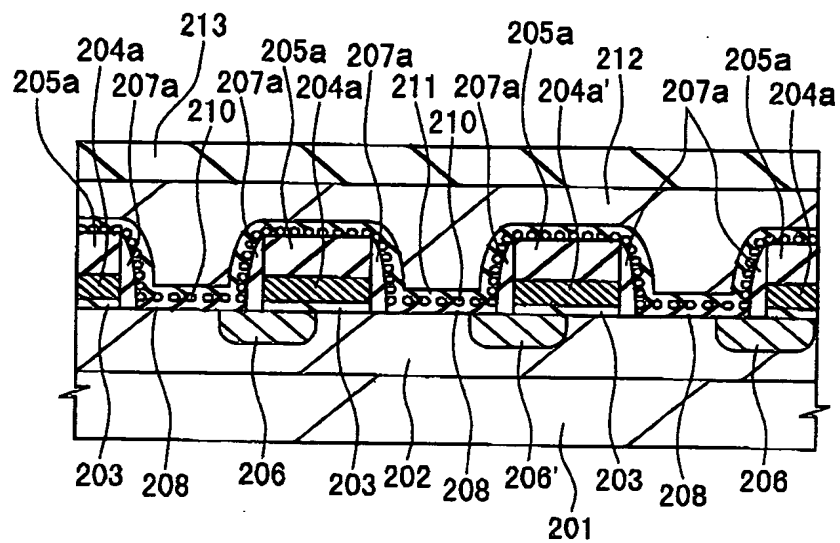


FIG. 20

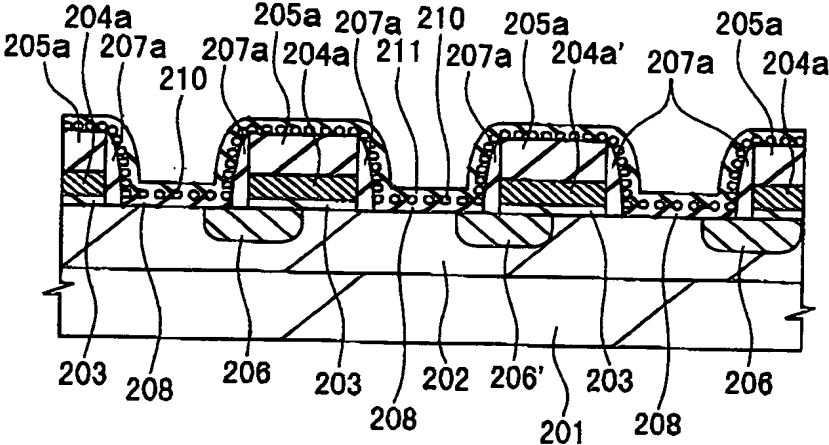
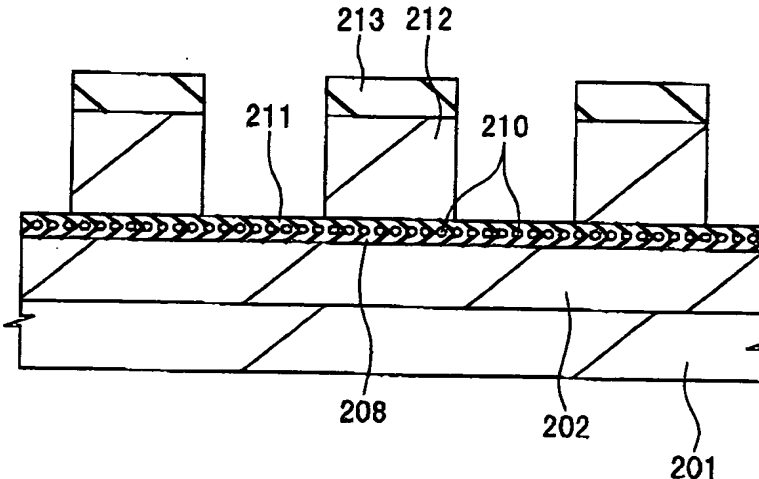


FIG.21



This diagram shows a cross-sectional view of the device during a programming operation. The word "PROGRAM" is written at the bottom. The structure is similar to the previous diagram, but with additional components and voltage levels. Labels include 213, 205a, 207a, 204a, 211, 210, 204a', 212, 202, 201, 206, A, 208, 206', 203, and 0V. Voltage levels are indicated at the top: 0V, 1.1V, 4.5V, and 8V. An arrow labeled "A" points to the right, indicating a direction of movement or a specific region.

[illegible]

FIG.24

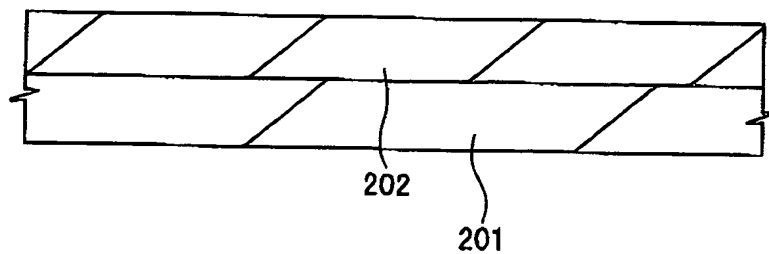


FIG.25

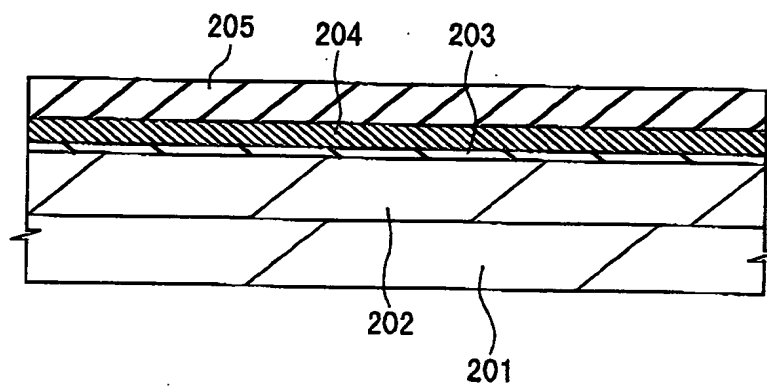


FIG.26

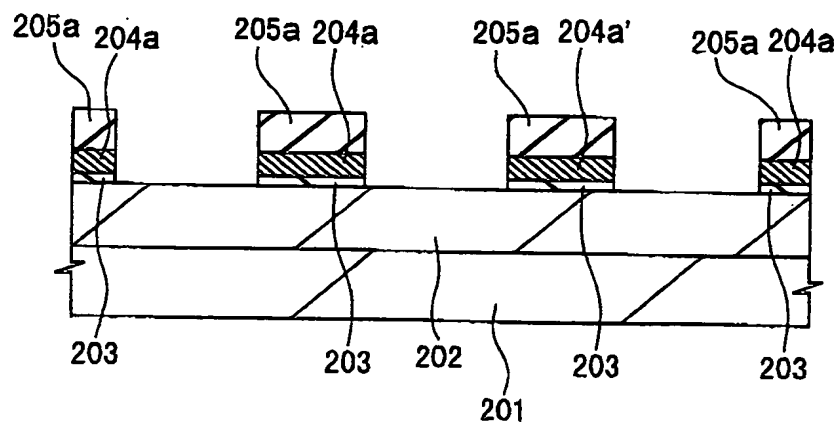


FIG.27

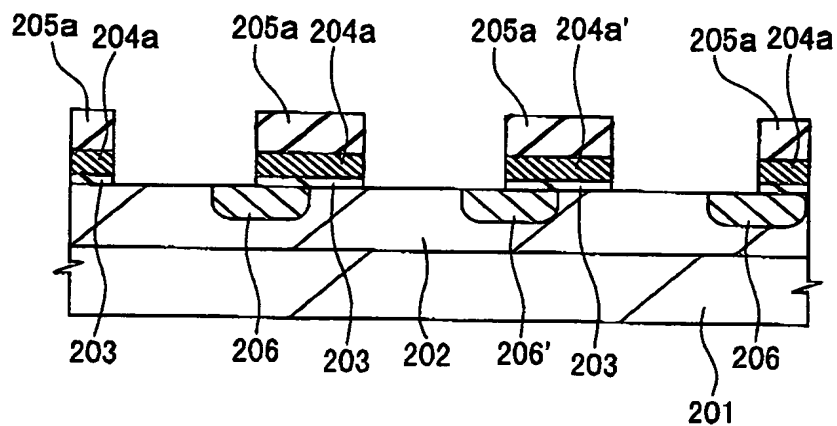


FIG.28

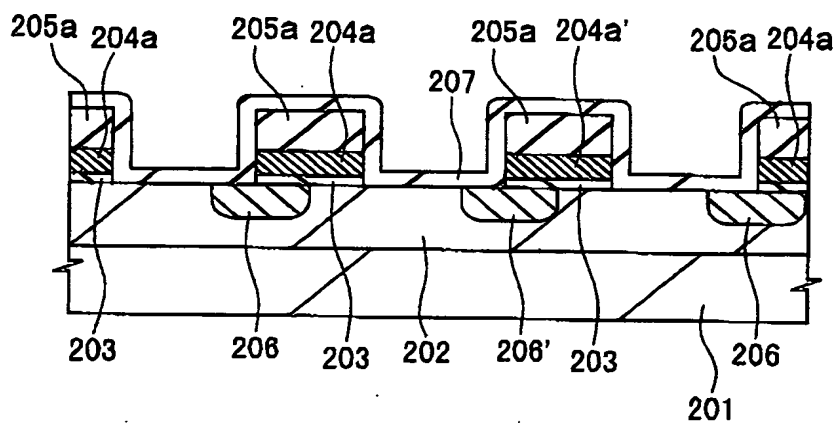


FIG.29

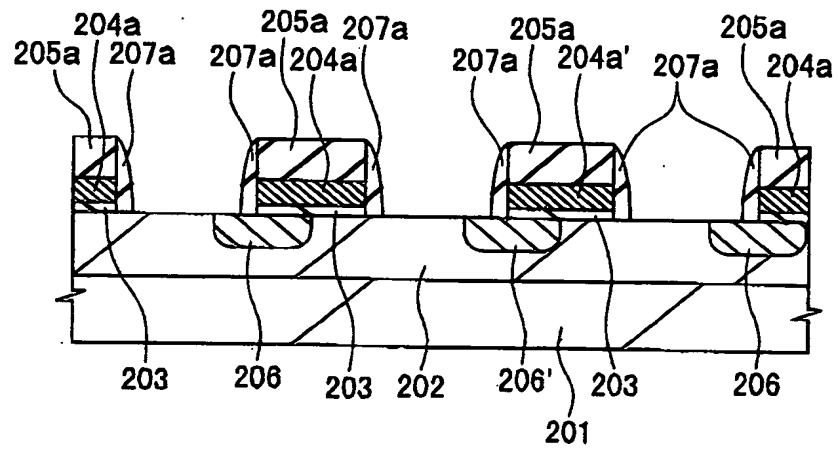
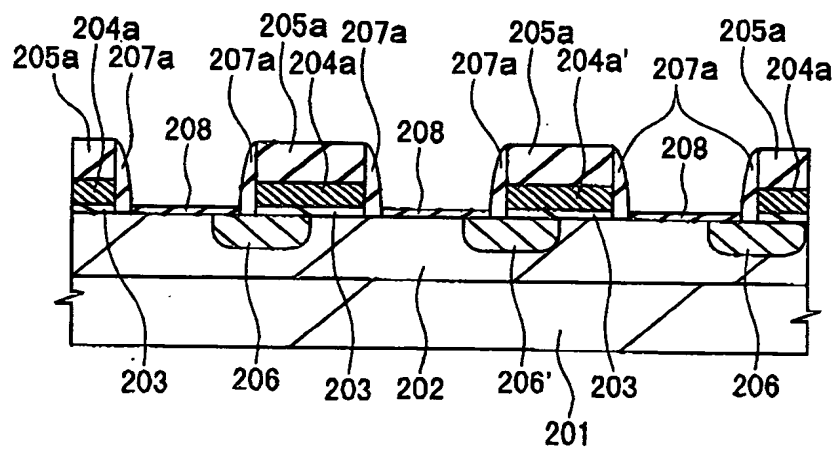


FIG.30



This cross-sectional view shows a semiconductor device with a substrate 201 and a base layer 202. Four repeating units are shown, each containing a gate stack 203, a gate electrode 204a, a gate insulating layer 205a, a gate contact 206, and a gate pad 207a. The gate stacks are separated by a gate spacer 208. The gate electrodes are connected to a common gate line 209. The gate insulating layer is connected to a common gate pad 209. The gate contacts are connected to a common gate contact 209. The gate pads are connected to a common gate pad 209. The gate spacers are connected to a common gate spacer 209. The gate electrodes are connected to a common gate line 209. The gate insulating layer is connected to a common gate pad 209. The gate contacts are connected to a common gate contact 209. The gate pads are connected to a common gate pad 209. The gate spacers are connected to a common gate spacer 209. The gate electrodes are connected to a common gate line 209. The gate insulating layer is connected to a common gate pad 209. The gate contacts are connected to a common gate contact 209. The gate pads are connected to a common gate pad 209. The gate spacers are connected to a common gate spacer 209.

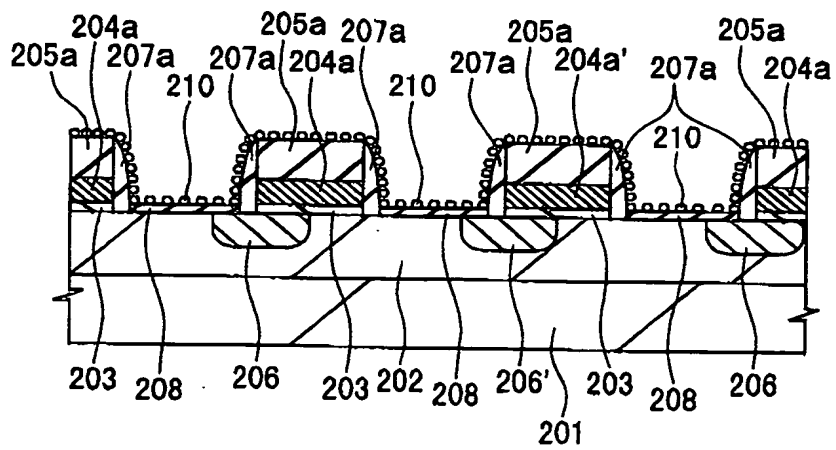


FIG.33

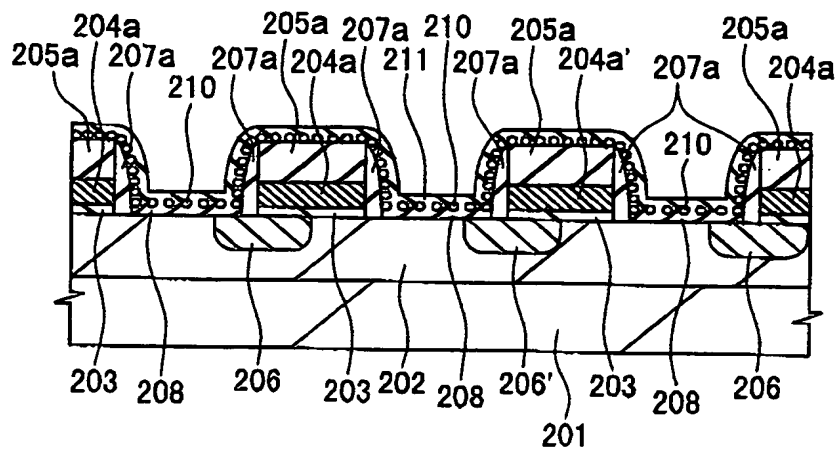


FIG.34

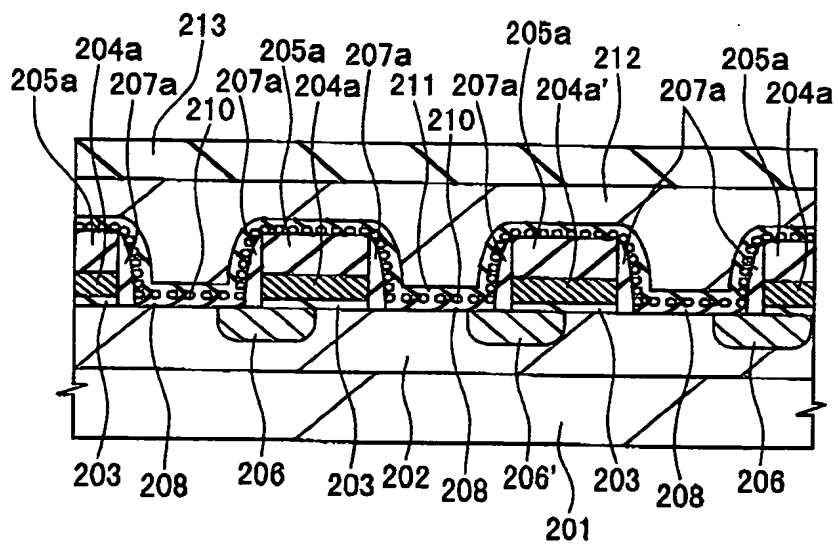


FIG.35

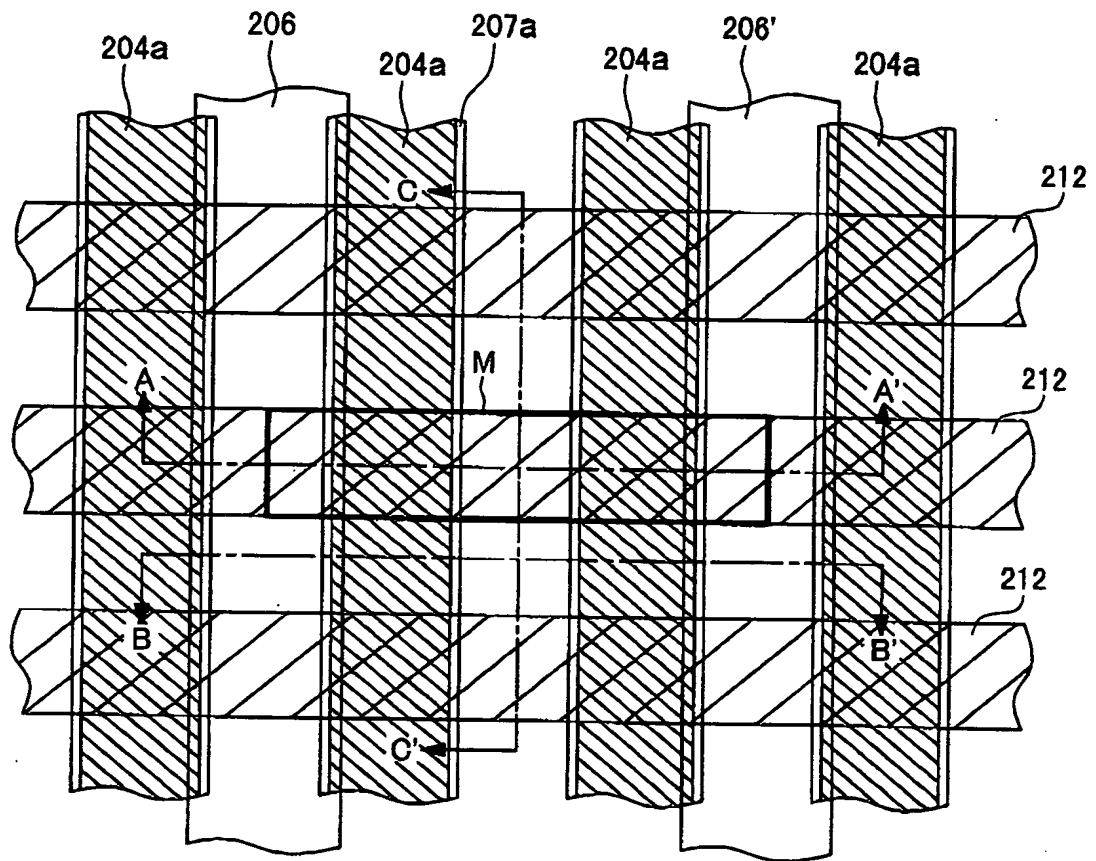


FIG.36

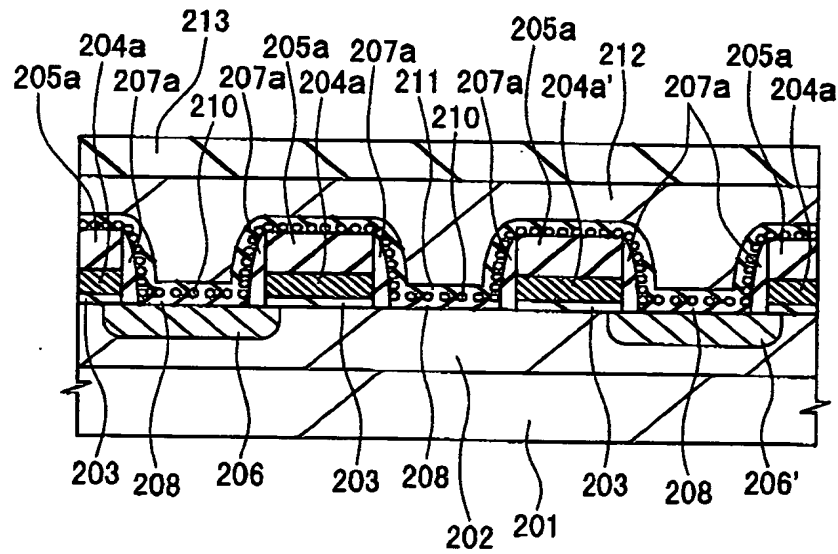


FIG.37

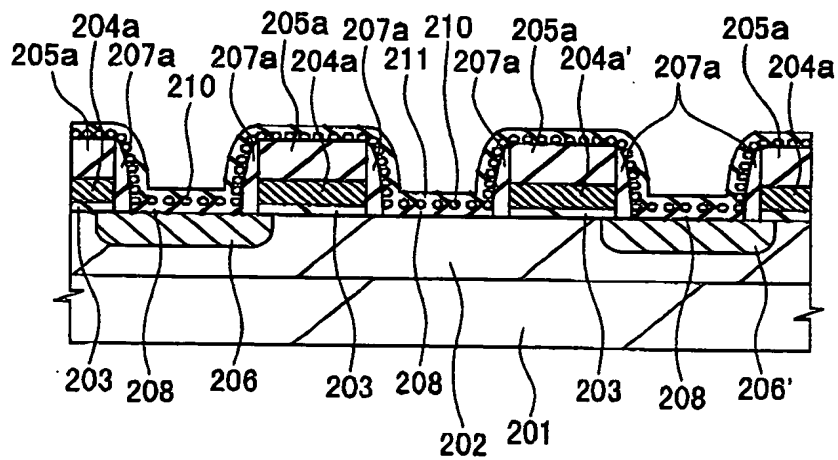


FIG.38

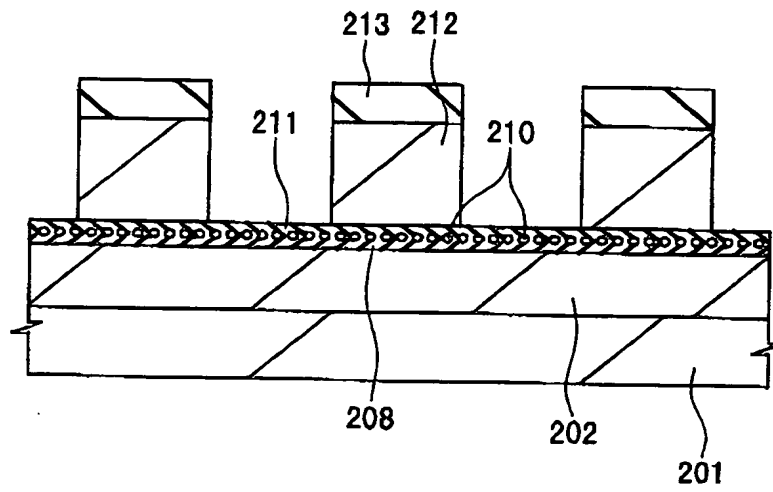


FIG.39

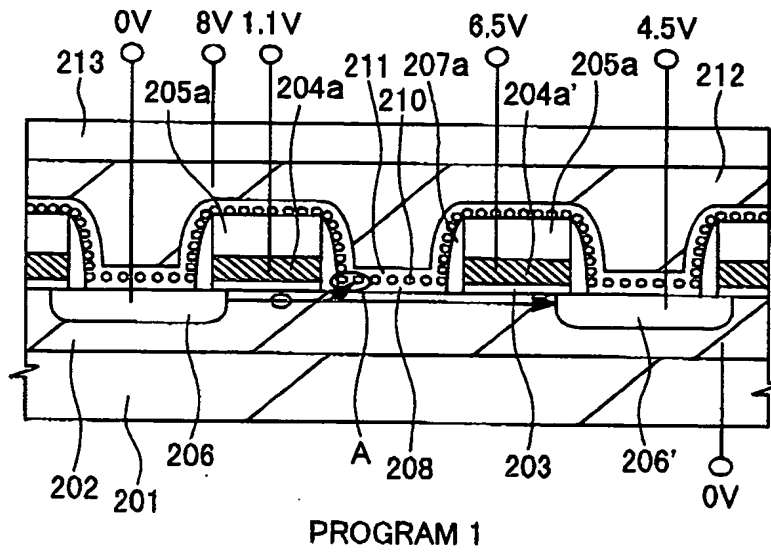


FIG.40

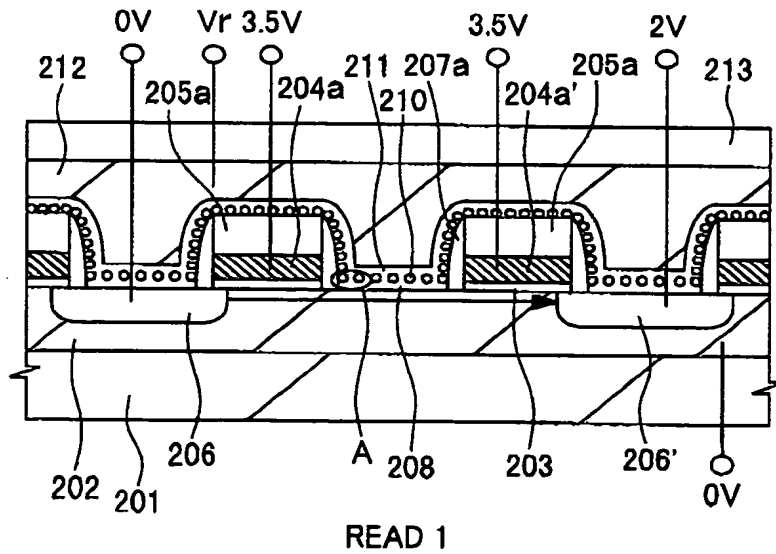


FIG.41

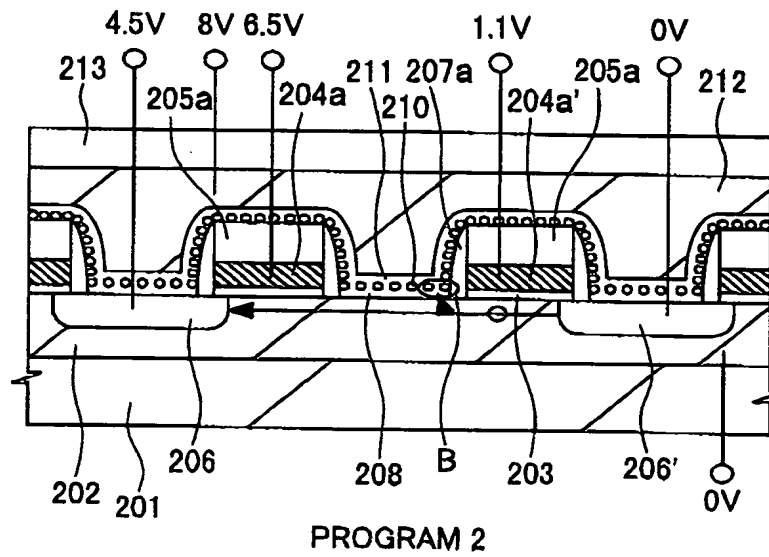


FIG.42

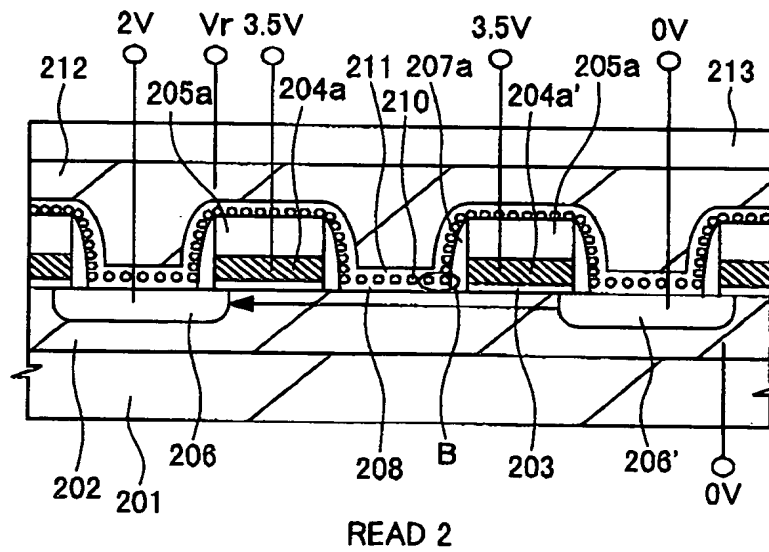


FIG.43

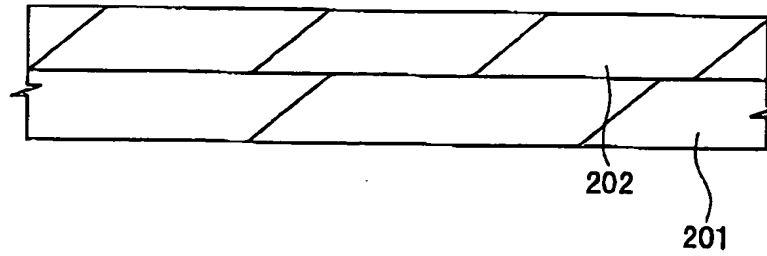


FIG.44

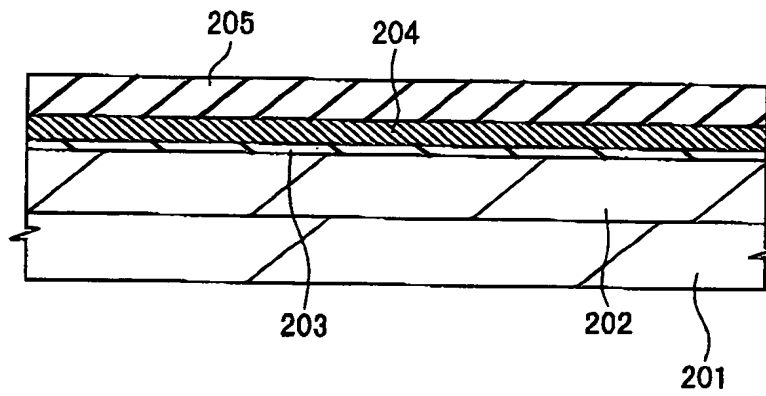


FIG.45

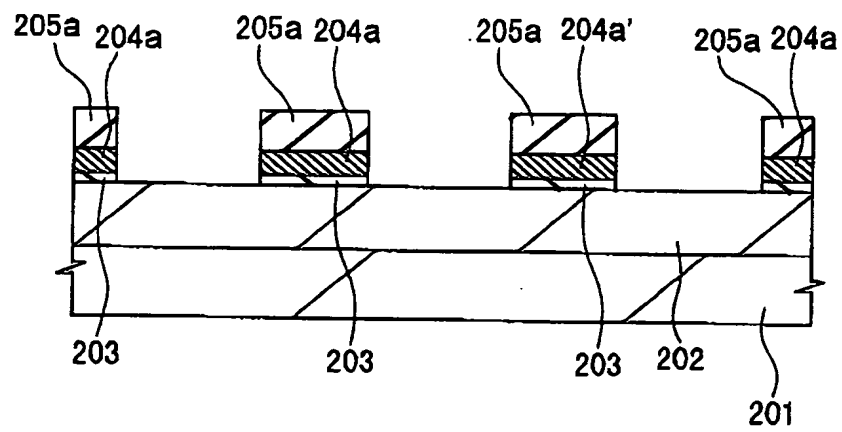


FIG.46

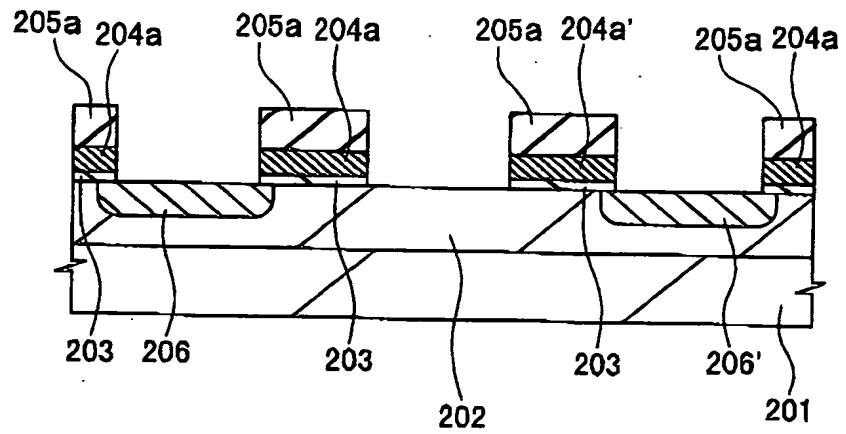


FIG.47

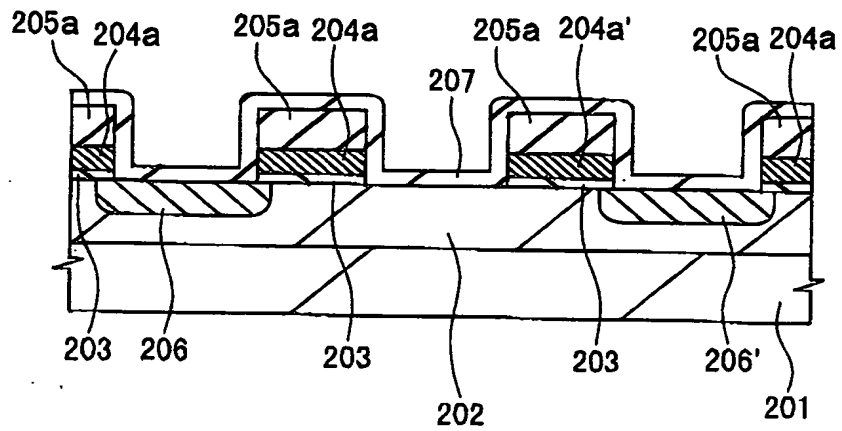


FIG.48

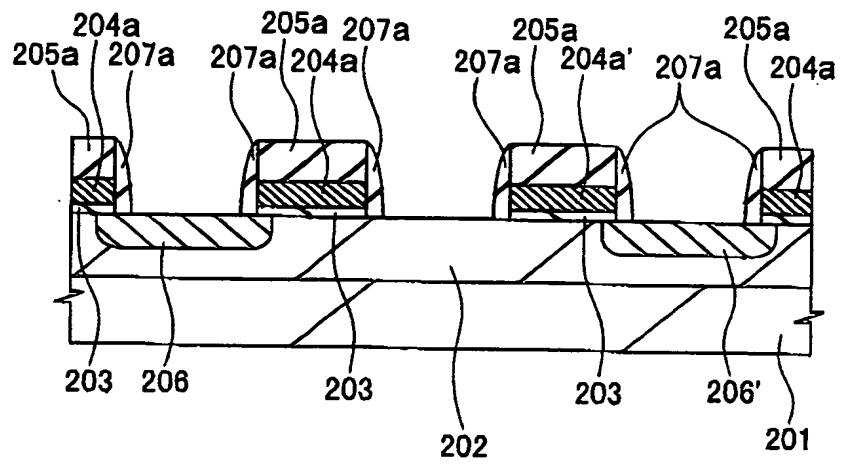
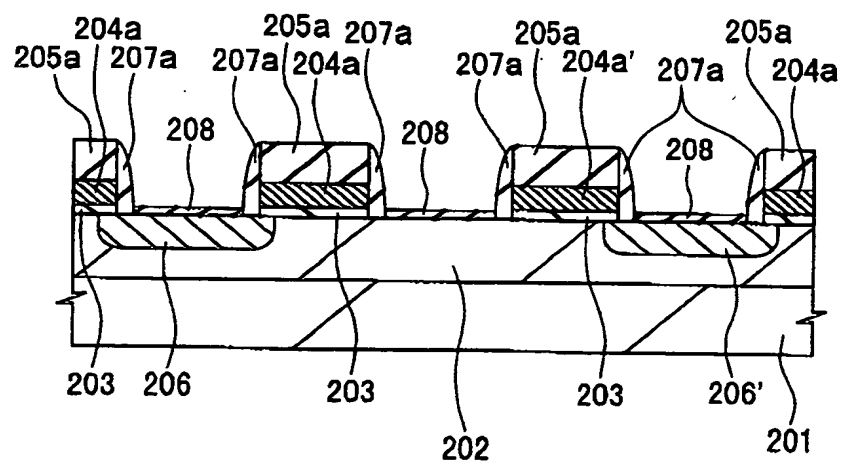


FIG.49



This cross-sectional diagram illustrates a semiconductor device with a substrate 201. A base layer 202 is formed on the substrate. Above the base layer, there are several gate structures. Each gate structure consists of a gate stack 209, which includes a gate dielectric layer 204a and a gate conductive layer 207a. The gate stacks are separated by side walls 206 and 206'. The regions between the gate stacks are labeled 203 and 208. The top surface of the gate conductive layer is indicated by 205a.

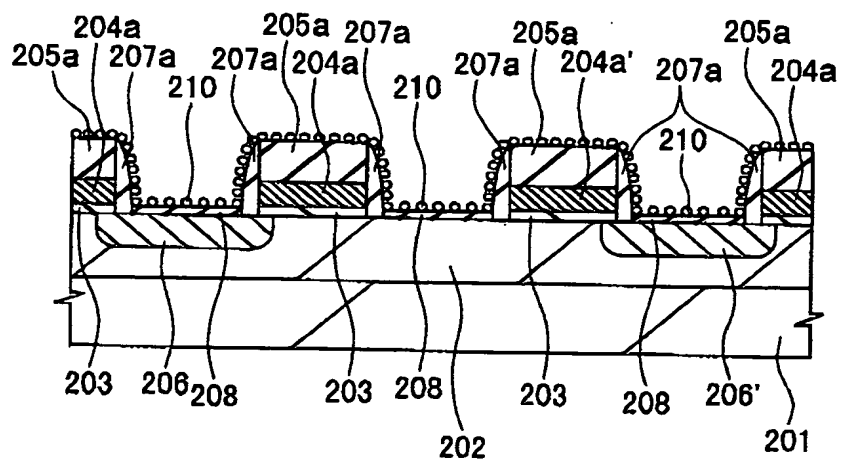


FIG.52

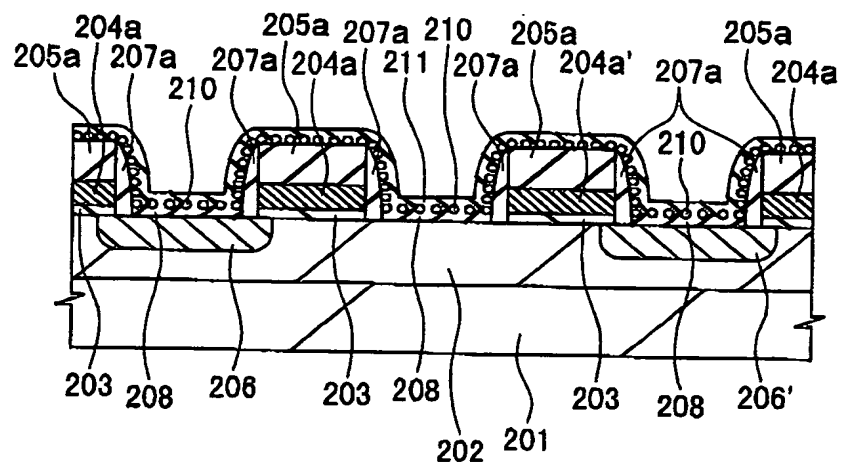


FIG.53

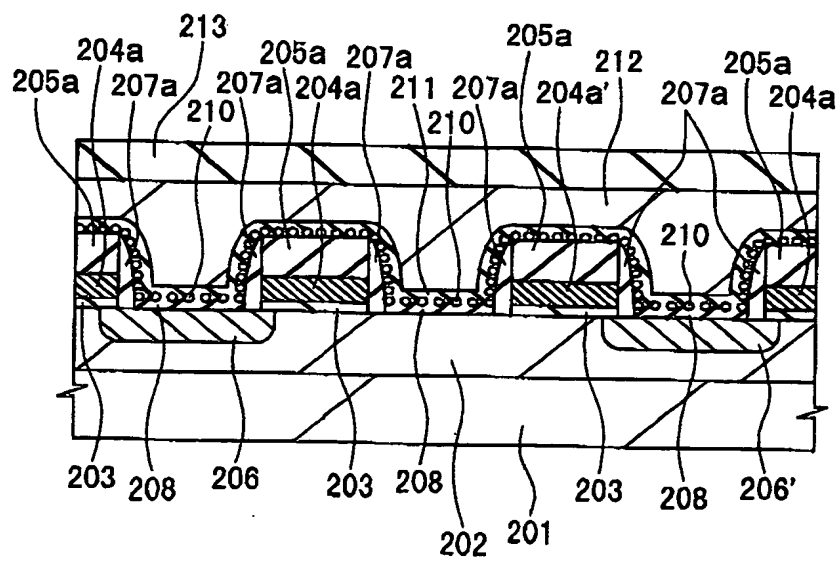


FIG.54

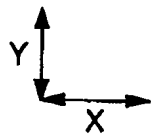
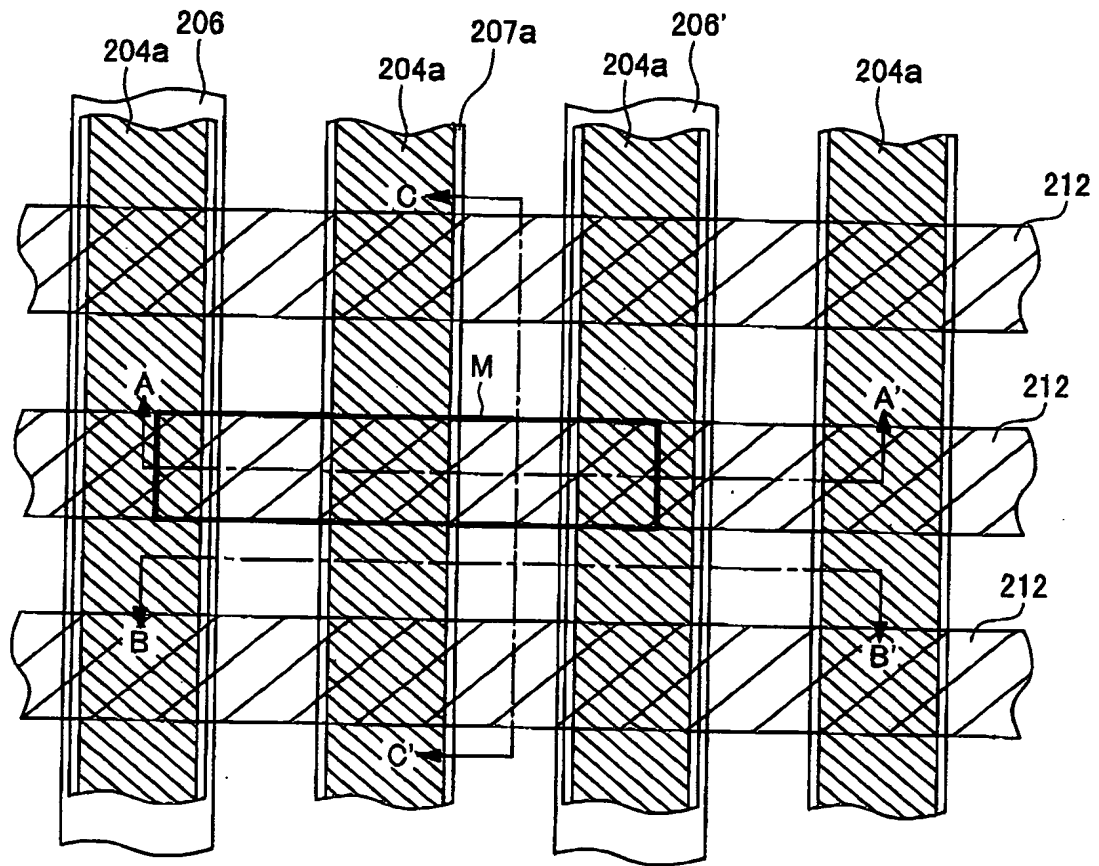


FIG.55

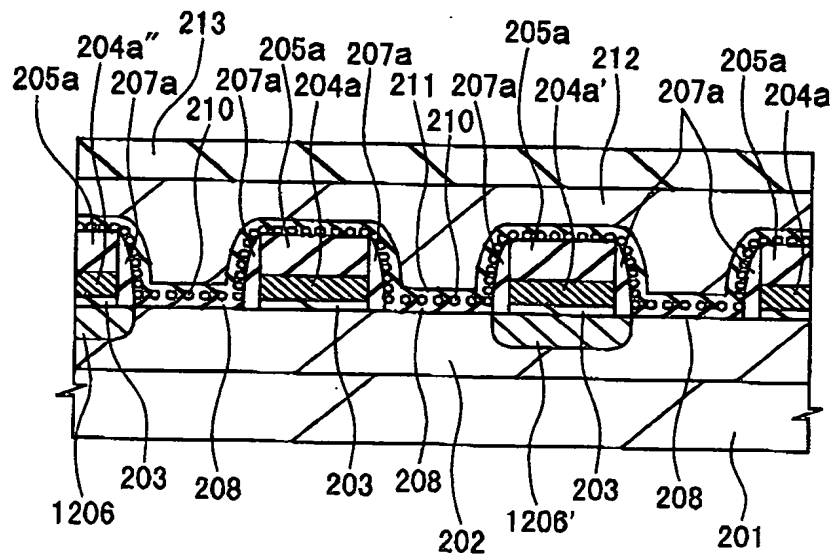


FIG.56

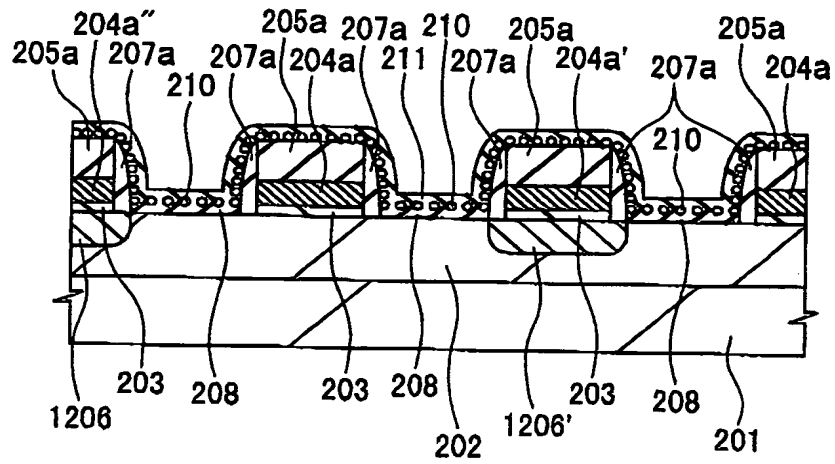


FIG.57

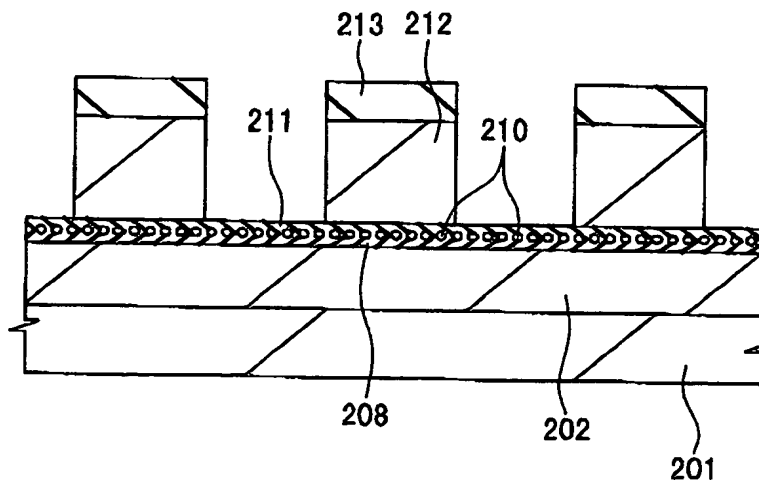


FIG.58

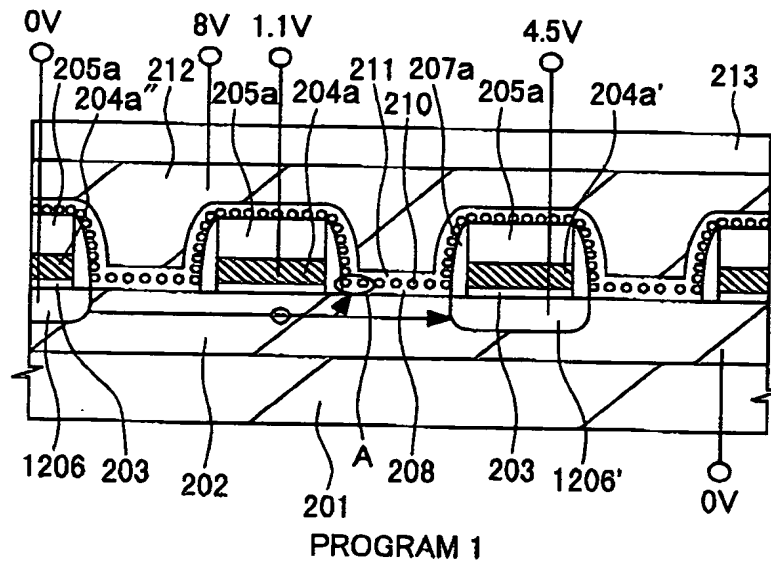


FIG.59

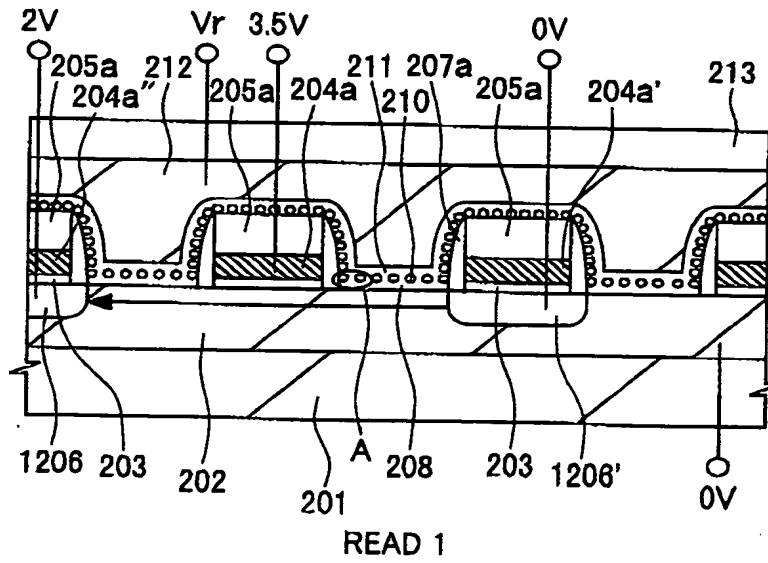


FIG.60

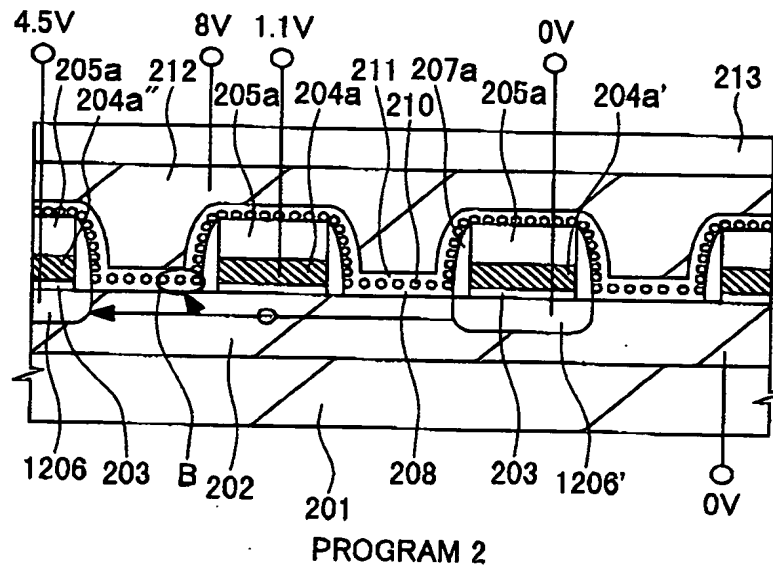


FIG.61

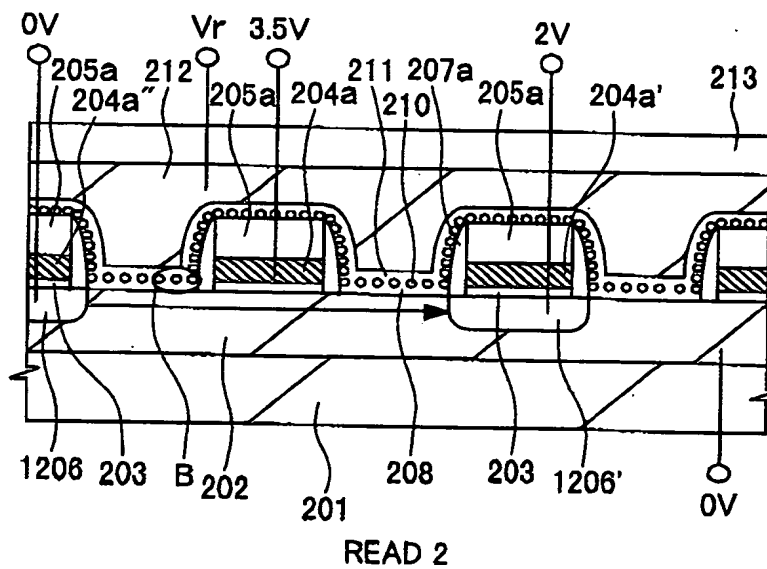


FIG.62

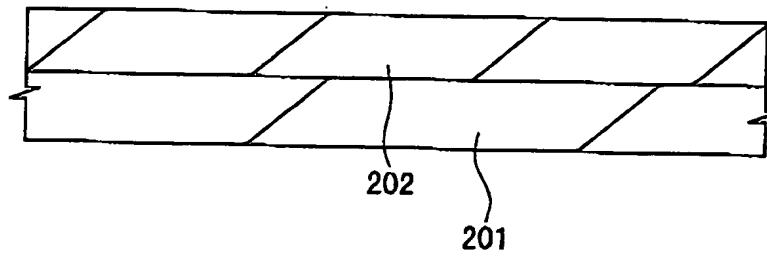


FIG.63

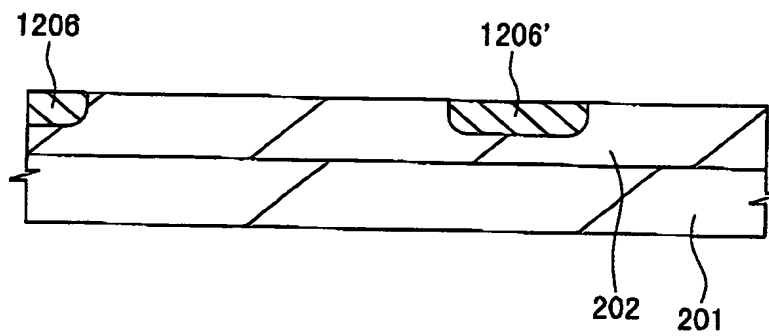


FIG.64

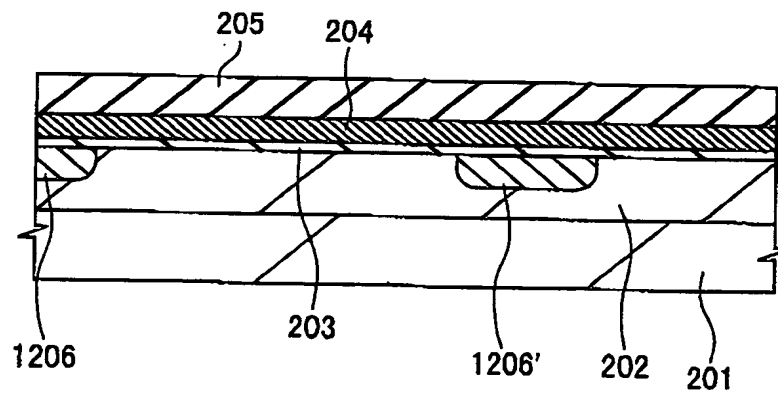


FIG.65

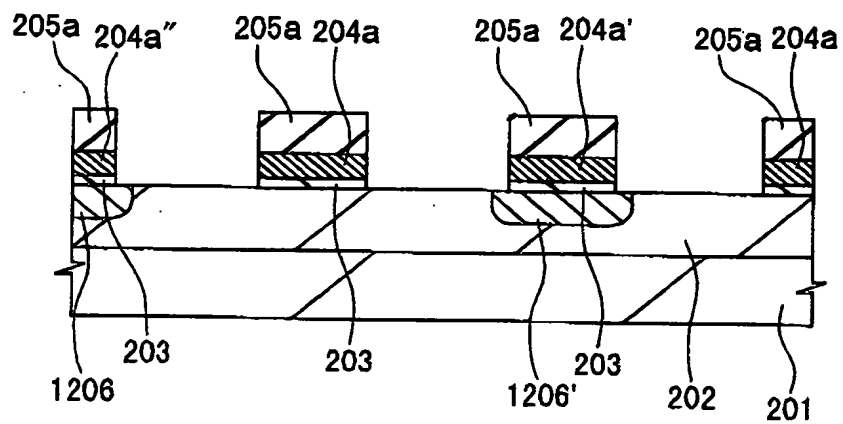
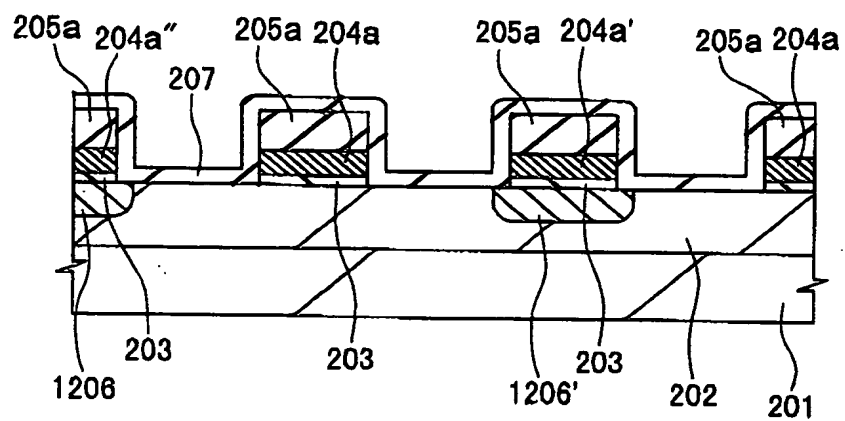


FIG.66



This cross-sectional view shows a substrate 201 with a top layer 202 and a bottom layer 203. Four solder bumps 205a are mounted on the top layer 202. The bumps are connected to a conductive layer 204a on the top layer and a conductive layer 204a' on the bottom layer 203. The bumps are also connected to a conductive layer 207a on the top layer. The bumps are labeled 204a'', 205a, 207a, 204a, 207a, 205a, 204a', 207a, 205a, 204a. The bumps are labeled 1206, 203, 203, 1206', 202, 201.

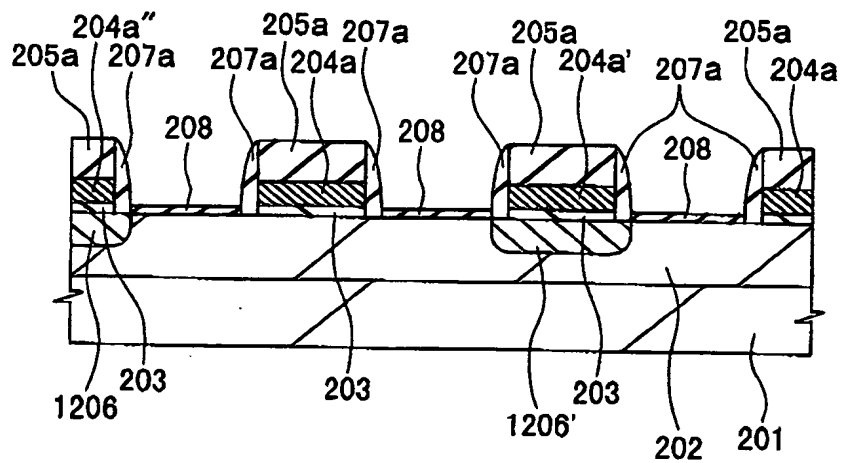
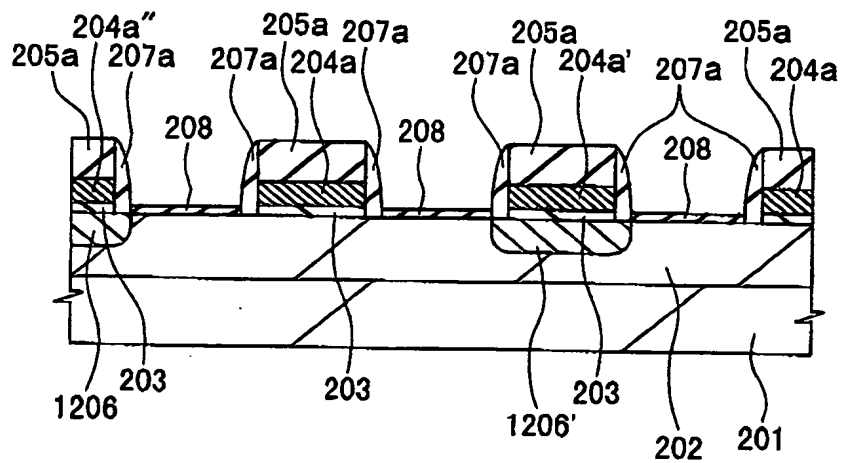


FIG.69

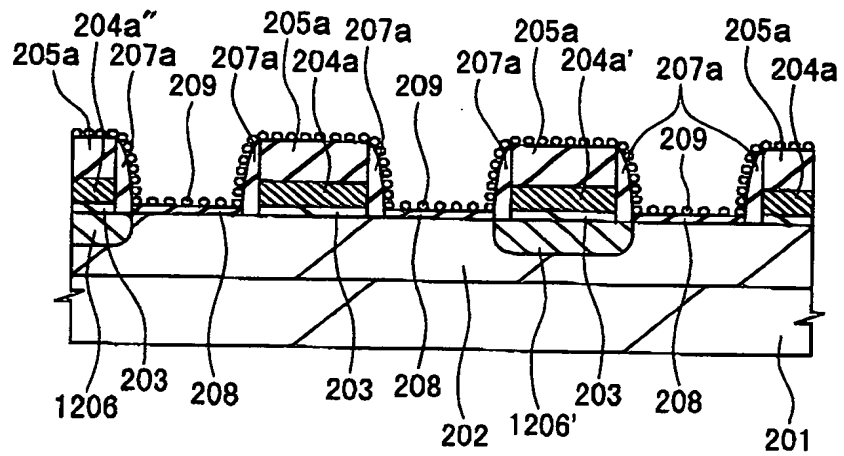


FIG.70

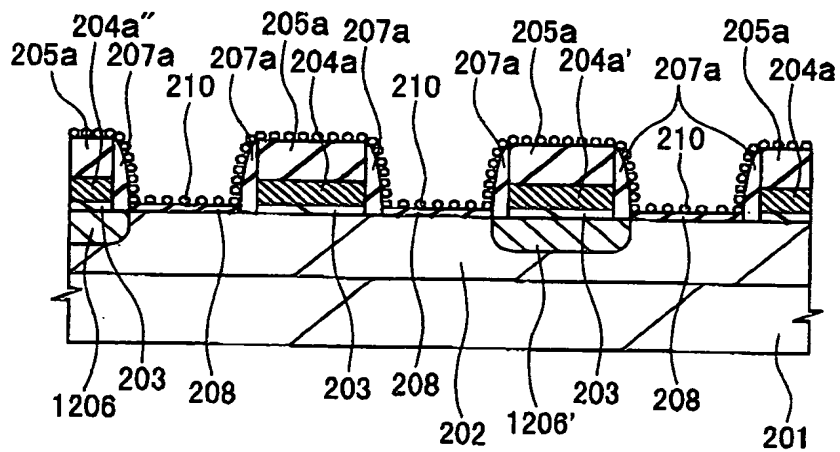


FIG.71

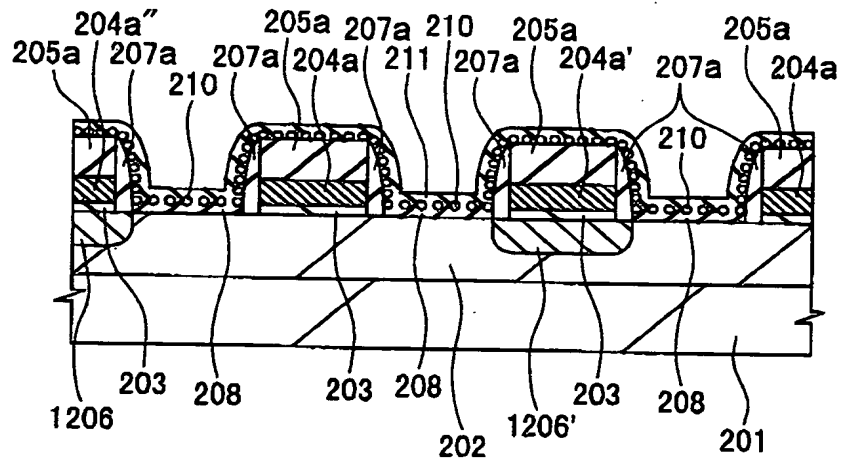


FIG.72

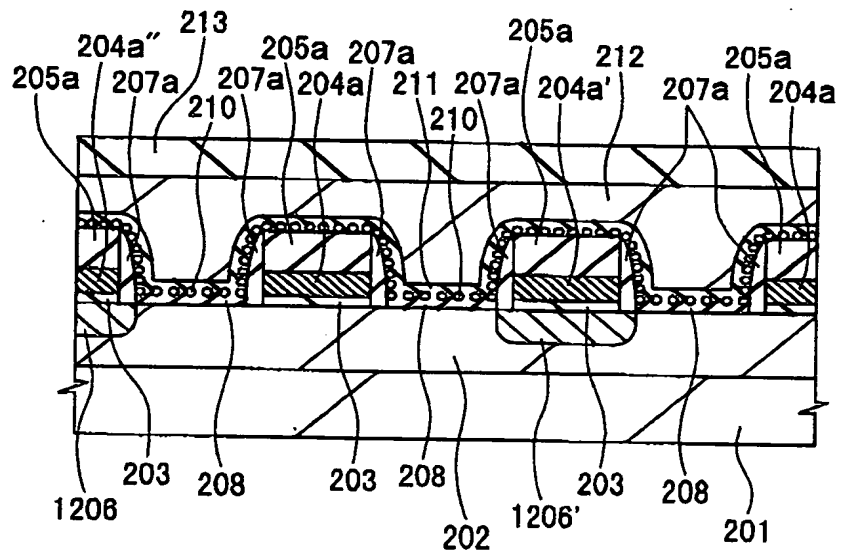


FIG.73

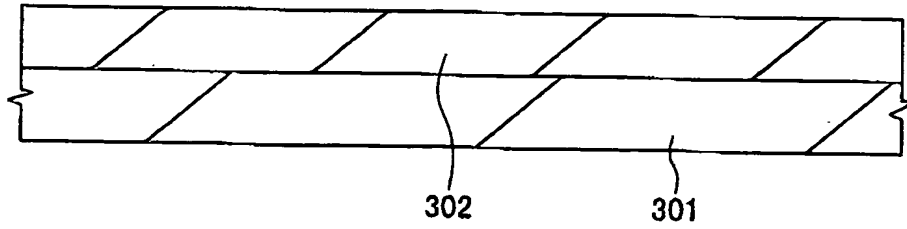


FIG.74

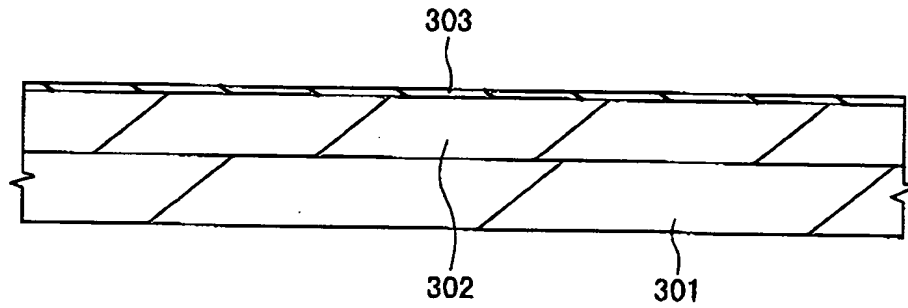


FIG.75

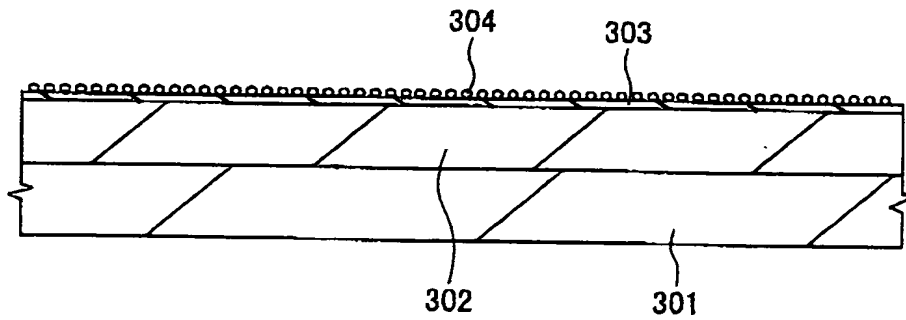


FIG.76

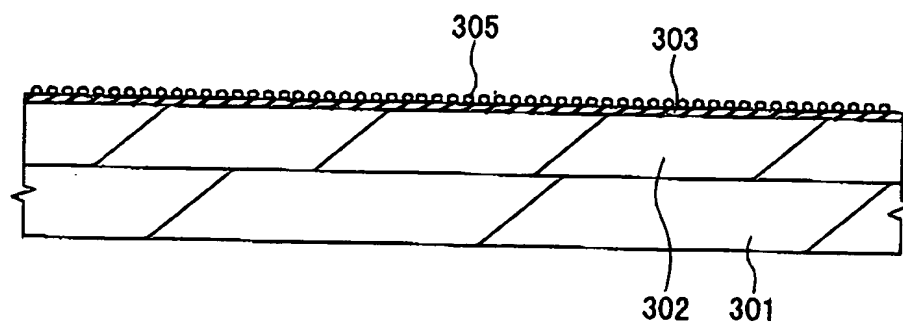


FIG.77

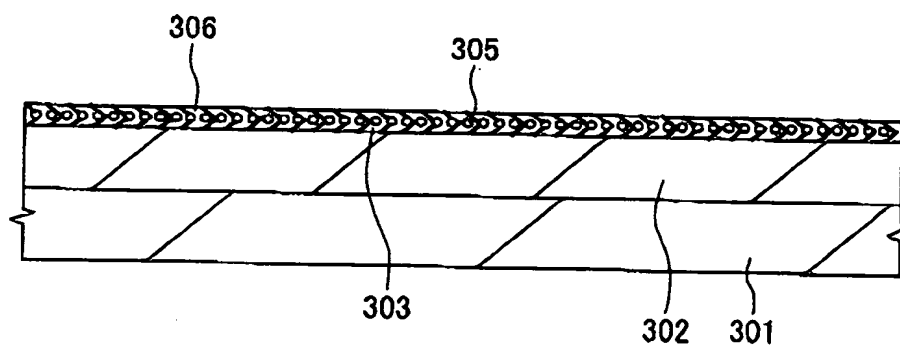


FIG.78

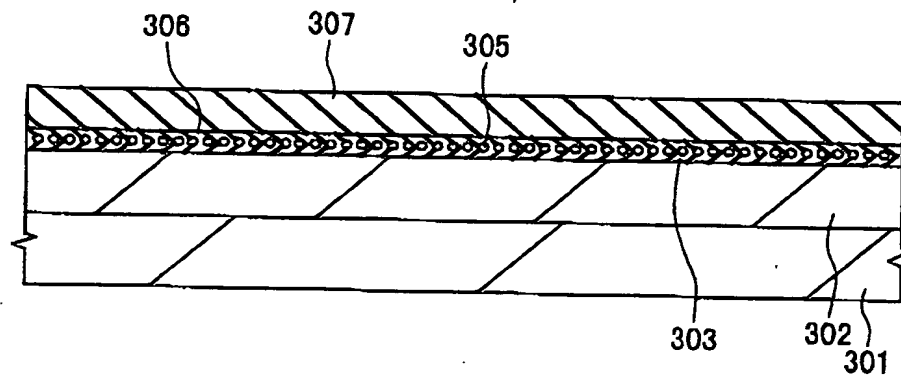


FIG.79

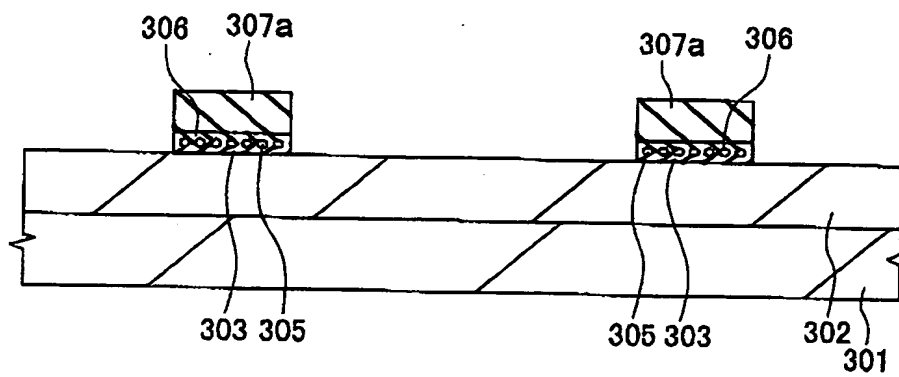


FIG.80

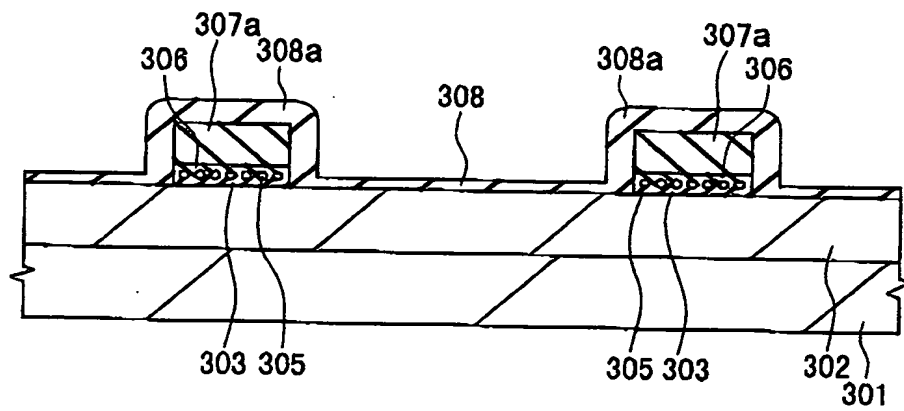


FIG.81

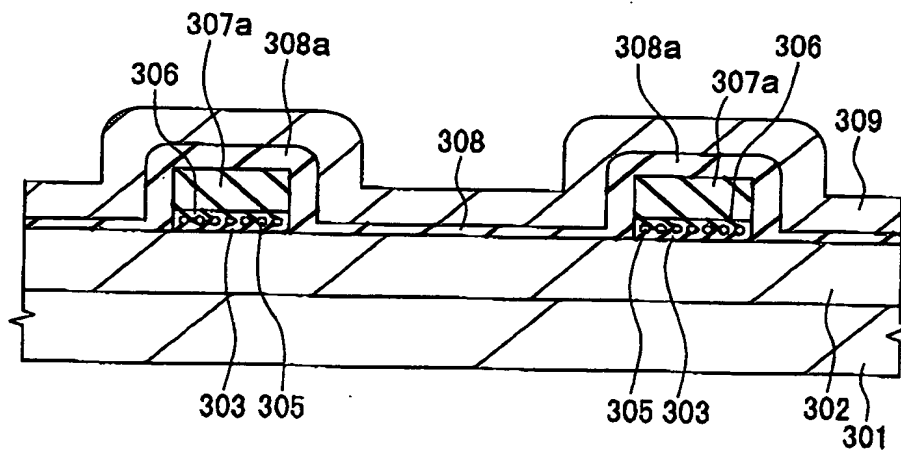


FIG.82

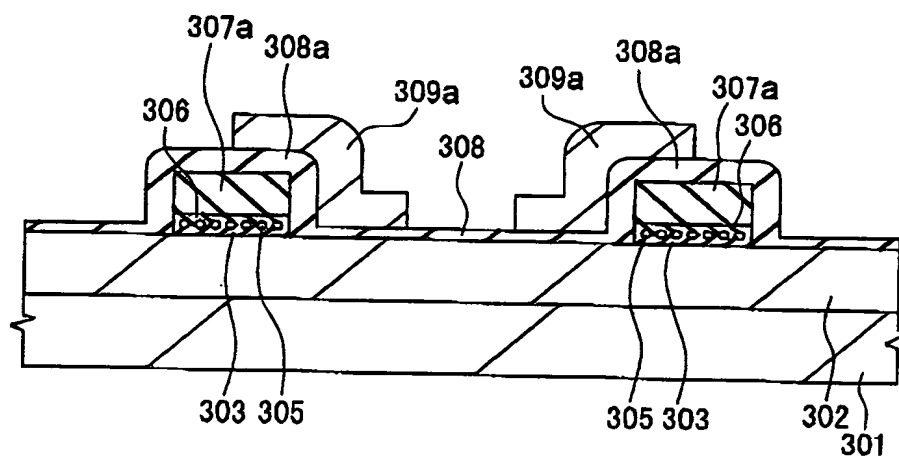


FIG.83

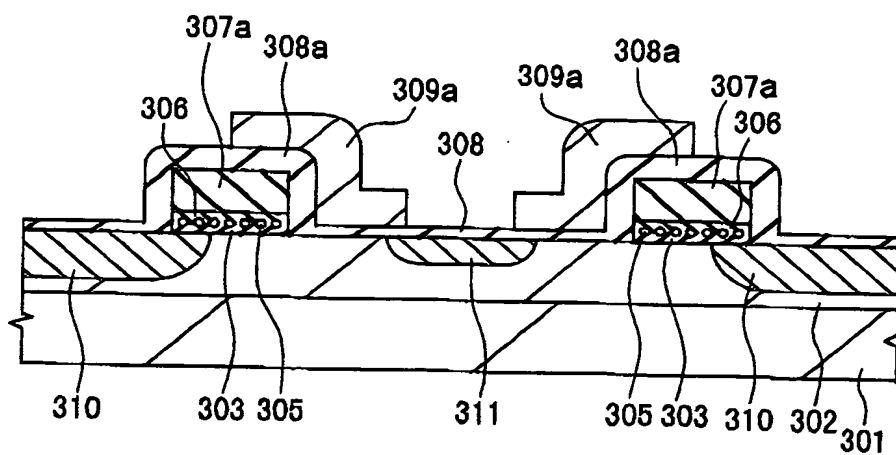


FIG.84

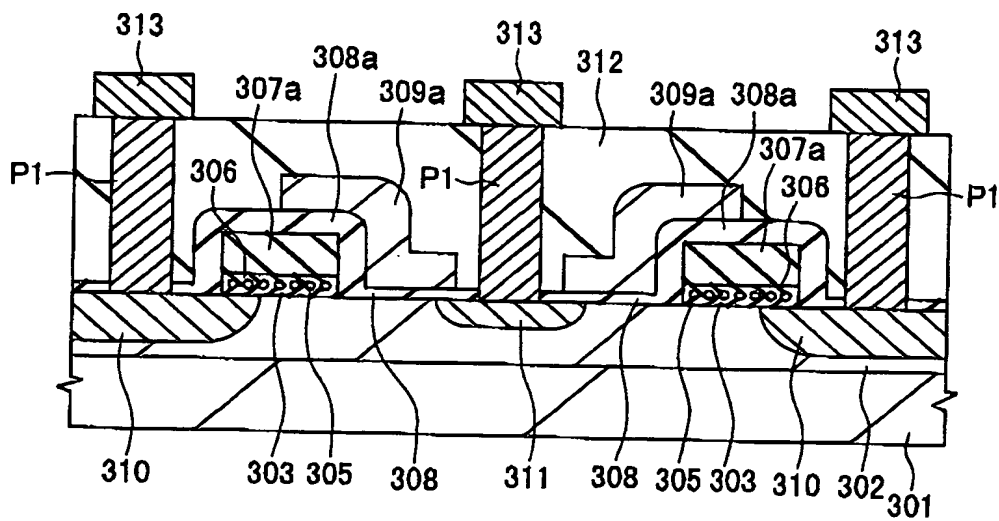


FIG.85

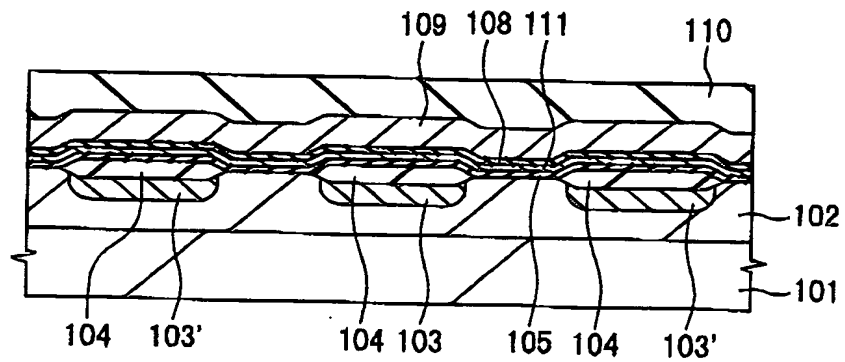
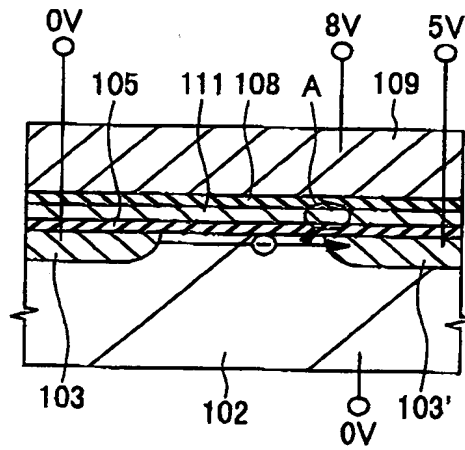
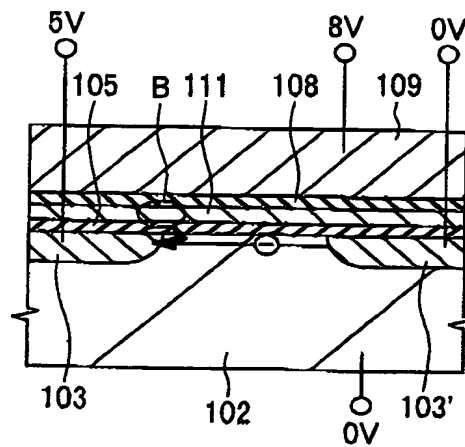


FIG.86



PROGRAM 1

FIG.87



PROGRAM 2

FIG.88

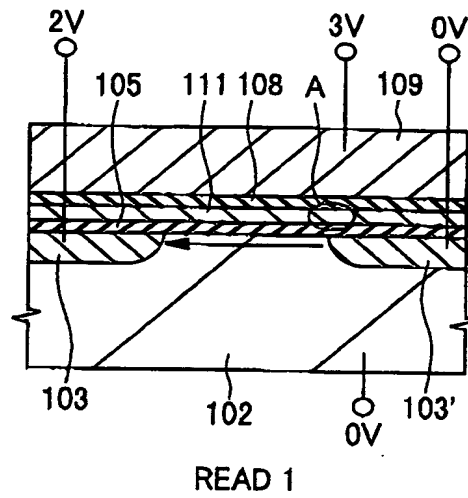


FIG.89

